CherryMote v5

schematics

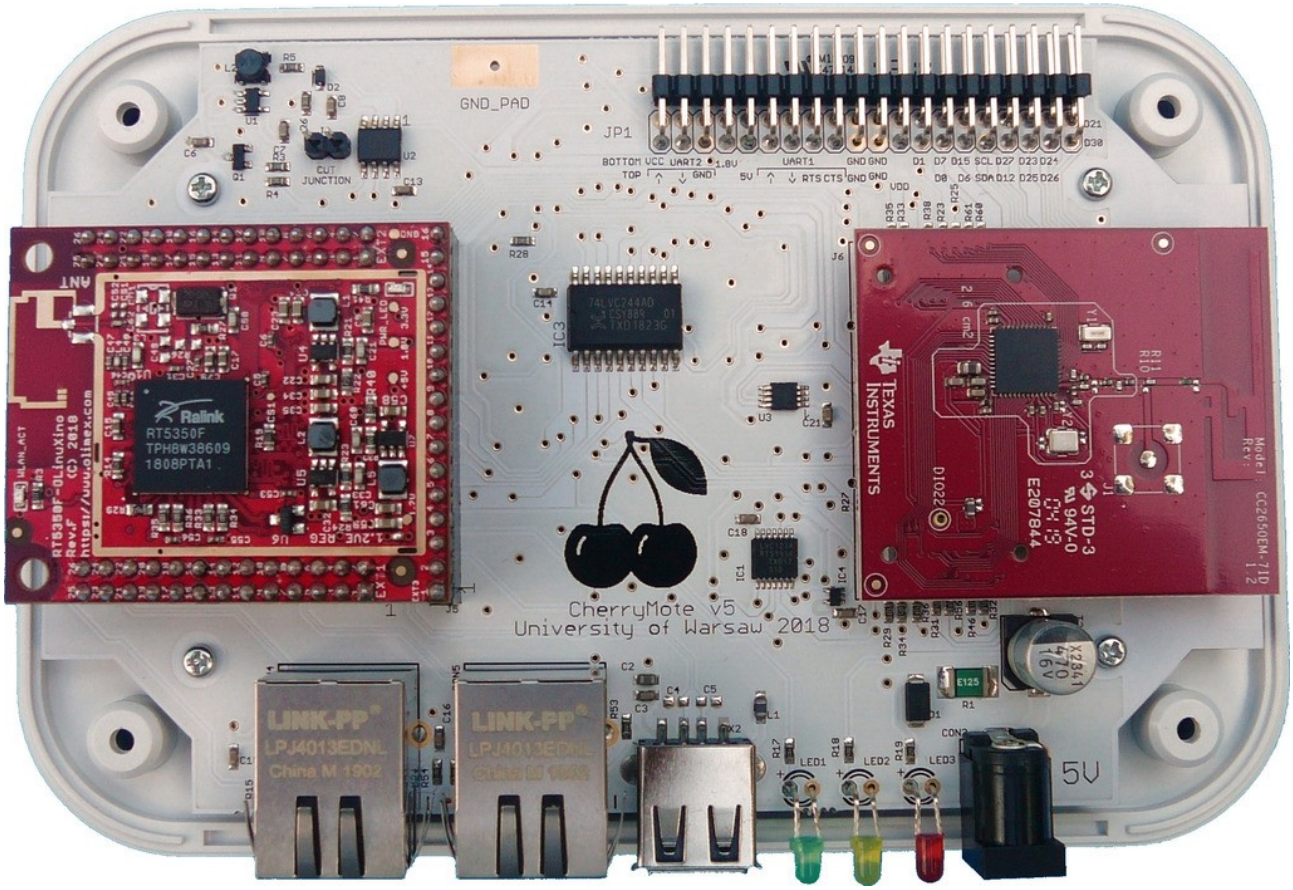
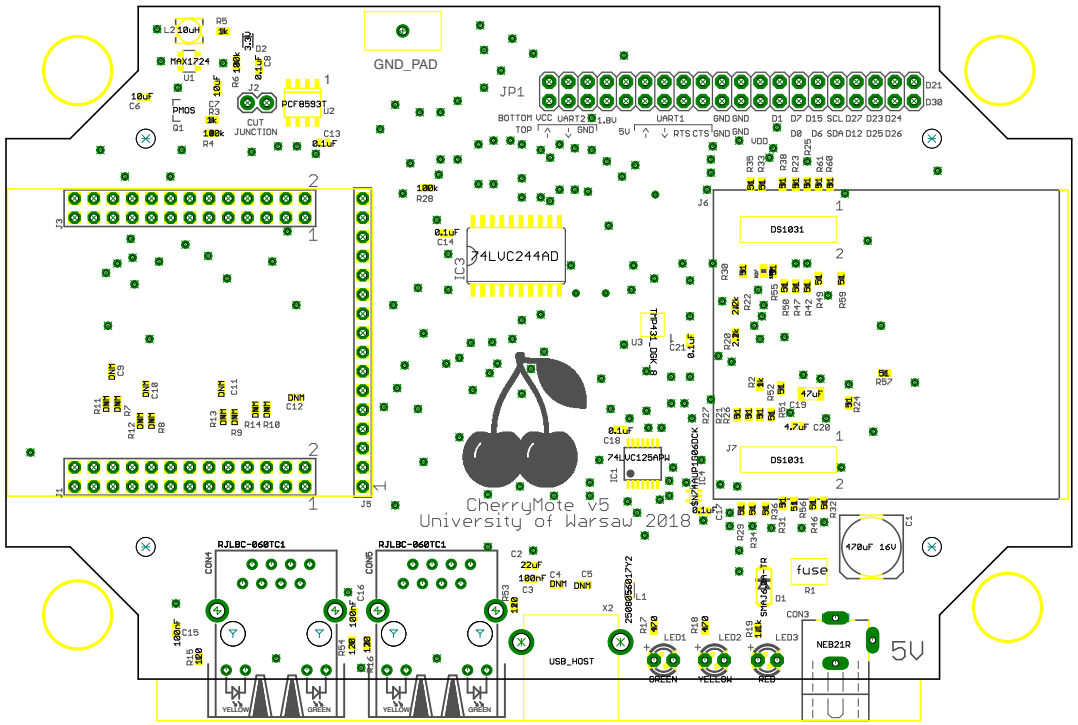
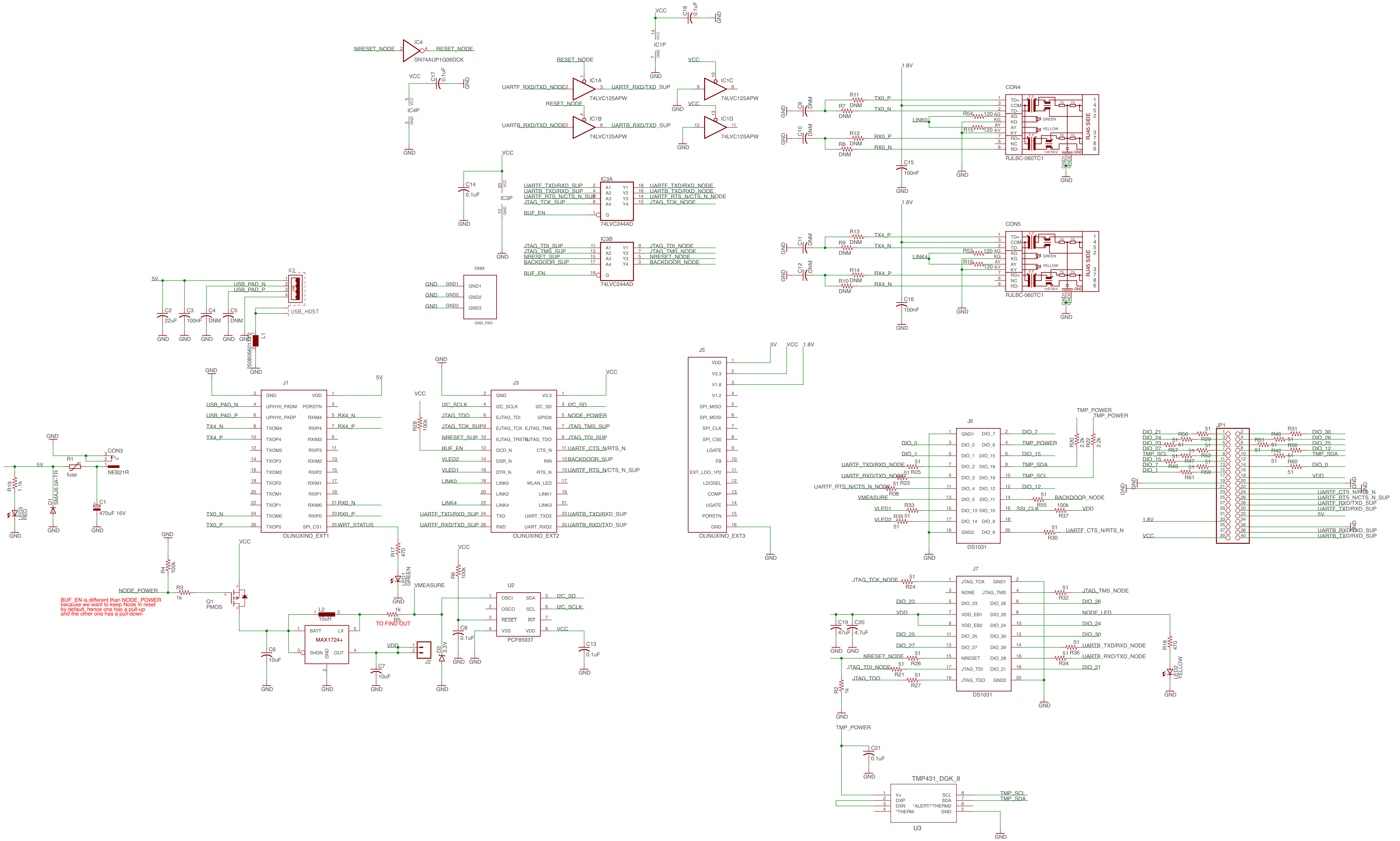


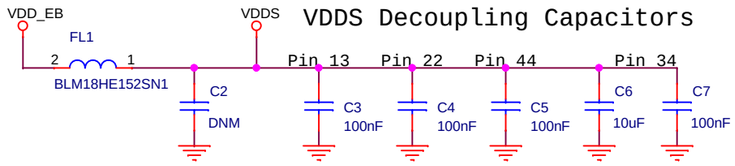
Table of contents:



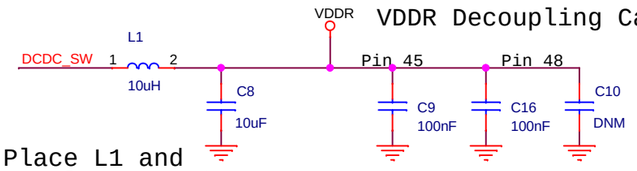
Sym	N°	Mils	MM	Qty	Plated
+	1	20	0.51	3	YES
×	2	24	0.60	181	YES
⊡	3	32	0.81	9	YES
◇	4	35	0.90	24	YES
⧖	5	39	1.00	68	YES
⋈	6	40	1.02	42	YES
ϟ	7	43	1.10	1	YES
ϟ	8	79	2.00	4	YES
✳	9	91	2.30	2	YES
✳	10	98	2.50	4	NOT
⍑	11	126	3.20	8	NOT



NRESET_NODE
RESET_NODE
IC4
SN74AUP1G06DCK
VCC
C17
0.1uF
GND
IC4P
C18
0.1uF
IC1P
RESET_NODE
IC1A
UARTF_RXD/TXD_NODE
UARTF_RXD/TXD_SUP
74LVC125APW
IC1B
UARTB_RXD/TXD_NODE
UARTB_RXD/TXD_SUP
IC1C
IC1D
C14
0.1uF
IC3P
IC3A
UARTF_TXD/RXD_SUP
UARTB_TXD/RXD_SUP
UARTF_RTS_N/CTS_N_SUP
JTAG_TCK_SUP
BUF_EN
UARTF_TXD/RXD_NODE
UARTB_TXD/RXD_NODE
UARTF_RTS_N/CTS_N_NODE
JTAG_TCK_NODE
74LVC244AD
IC3B
JTAG_TDI_SUP
JTAG_TMS_SUP
NRESET_SUP
BACKDOOR_SUP
JTAG_TDI_NODE
JTAG_TMS_NODE
NRESET_NODE
BACKDOOR_NODE
DNM
GND_PAD
1.8V
CON4
TX0_P
TX0_N
RX0_P
RX0_N
LINK0
RJLBC-060TC1
RJ45 SIDE
GREEN
YELLOW
C15
100nF
CON5
TX4_P
TX4_N
RX4_P
RX4_N
LINK4
C16
100nF
5V
X2
USB_PAD_N
USB_PAD_P
USB_HOST
C2
22uF
C3
100nF
C4
C5
L1
J1
OLINUXINO_EXT1
J3
OLINUXINO_EXT2
J5
OLINUXINO_EXT3
I2C_SCLK
I2C_SD
NODE_POWER
UARTF_CTS_N/RTS_N
UARTF_RTS_N/CTS_N_SUP
VLED2
VLED1
WRT_STATUS
R28
100k
CON3
R1
fuse
NEB21R
R19
1.1k
LED3
RED
D1
SMAJ6.0A-TR
C1
470uF 16V
R4
100k
R3
1k
Q1
PMOS
BUF_EN is different than NODE_POWER because we want to keep Node in reset by default, hence one has a pull-up and the other one has a pull-down
C6
10uF
L2
10uH
MAX1724+
C7
10uF
R5
1k
TO FIND OUT
VMEASURE
R17
470
LED1
GREEN
J2
D2
3.3V
R6
100k
C8
0.1uF
U2
PCF8593T
C13
0.1uF
J6
DS1031
TMP_POWER
TMP_SDA
TMP_SCL
SSI_CLK
R20
R22
2.2k
JP1
J7
JTAG_TCK_NODE
JTAG_TMS_NODE
NODE_LED
C19
47uF
C20
4.7uF
R2
1k
R18
470
LED2
YELLOW
C21
0.1uF
TMP431_DGK_8
U3

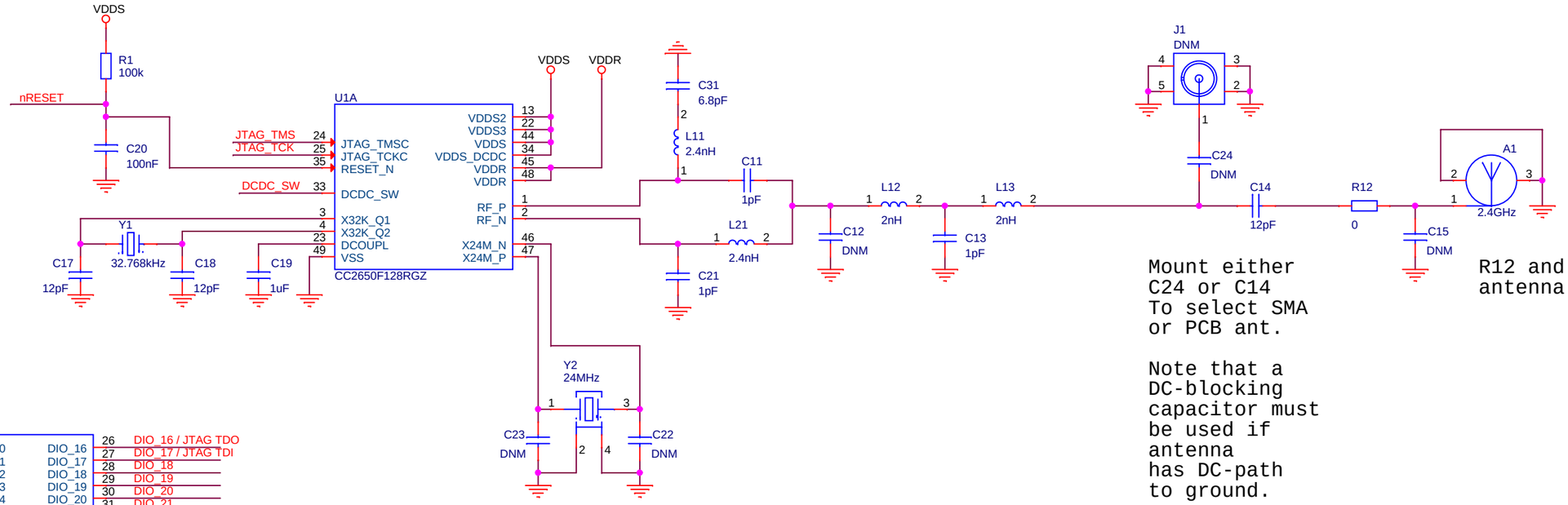


VDDS Decoupling Capacitors



VDDR Decoupling Capacitors

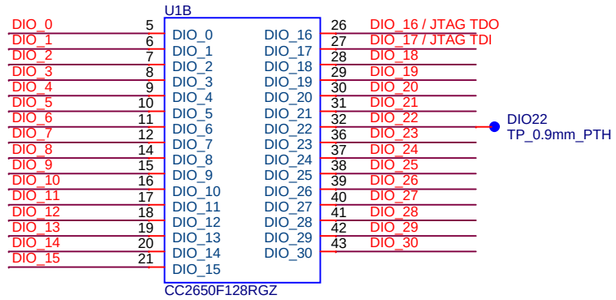
Place L1 and
C8 close to pin 33



Mount either
C24 or C14
To select SMA
or PCB ant.

Note that a
DC-blocking
capacitor must
be used if
antenna
has DC-path
to ground.

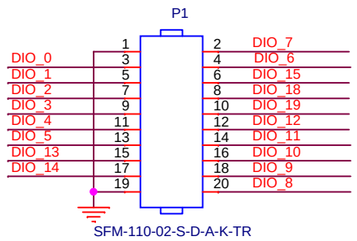
R12 and C15 for
antenna matching



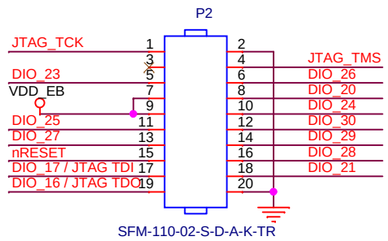
NOTE:
The CC2650 is a superset of CC2610, CC2620, CC2630 and CC2640. This design can thus be considered a reference design for all of these devices.

Likewise, the CC2650EM board can be used to evaluate the performance for all the above mentioned devices.

EM connector 1

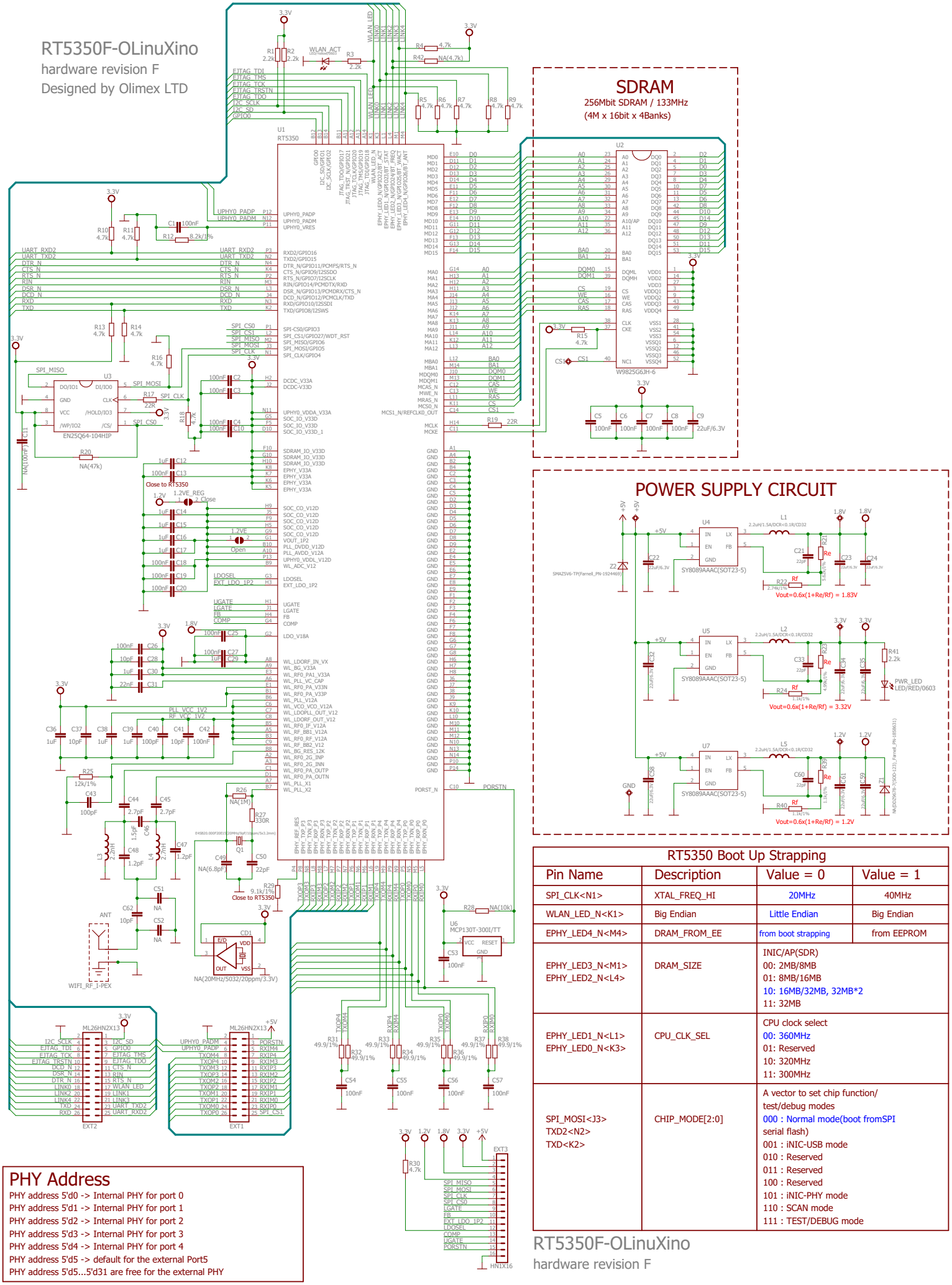


EM connector 2



FIDU1 FIDU2 FIDU3
FIDU4 FIDU5 FIDU6

Title:	CC2650EM-7ID
Drawn:	FGK
Checked:	
Size: A3	Rev: 1.2.6
Sheet:	1 of 1
Date:	Thursday, February 05, 2015



RT5350 Boot Up Strapping

Pin Name	Description	Value = 0	Value = 1
SPI_CLK<N1>	XTAL_FREQ_HI	20MHz	40MHz
WLAN_LED_N<K1>	Big Endian	Little Endian	Big Endian
EPHY_LED4_N<M4>	DRAM_FROM_EE	from boot strapping	from EEPROM
EPHY_LED3_N<M1> EPHY_LED2_N<L4>	DRAM_SIZE	INIC/AP(SDR) 00: 2MB/8MB 01: 8MB/16MB 10: 16MB/32MB, 32MB*2 11: 32MB	
EPHY_LED1_N<L1> EPHY_LED0_N<K3>	CPU_CLK_SEL	CPU clock select 00: 360MHz 01: Reserved 10: 320MHz 11: 300MHz	
SPI_MOSI<J3> TXD2<N2> TXD<K2>	CHIP_MODE[2:0]	A vector to set chip function/ test/debug modes 000 : Normal mode(boot fromSPI serial flash) 001 : iNIC-USB mode 010 : Reserved 011 : Reserved 100 : Reserved 101 : iNIC-PHY mode 110 : SCAN mode 111 : TEST/DEBUG mode	

RT5350F-OLinuXino
hardware revision F